THE INVENTION CLAIMED IS:

1. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising the steps of:

forming a multi-layer structure on an active region on the semiconductor substrate;

forming sidewall spacers around the multi-layer structure;

forming a dielectric layer over the semiconductor substrate, including the multi-layer structure, the sidewall spacers, and the active region;

forming a photoresist over the dielectric layer;

patterning and developing the photoresist to form a photoresist contact opening therein;

forming a tapered contact opening, using the photoresist contact opening, into the dielectric layer;

removing the photoresist; and

forming a conductive material in the tapered contact opening to form a contact in contact with the active region.

2. The method as claimed in claim 1 including a step of forming a bottom anti-reflecting coating on the dielectric layer before forming the photoresist over the dielectric layer to assist in patterning the photoresist.

3. The method as claimed in claim 1 including forming a bottom anti-reflective coating on the dielectric layer and forming a tapered opening therein which is used in forming the tapered contact opening.

4. The method as claimed in claim 1 wherein forming a tapered contact opening uses an etching process.

5. The method as claimed in claim 1 wherein forming a conductive material includes: depositing the conductive metal over the dielectric layer and in the tapered contact opening; and planarizing the conductive metal flush with the dielectric layer.

6. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming a multi-layer structure on an active region on the semiconductor substrate;

forming sidewall spacers around the multi-layer structure;

implanting source and drain regions in the active region adjacent the sidewall spacers;

depositing a dielectric liner layer of silicon nitride over the semiconductor substrate, in contact with the multi-layer structure, the sidewall spacers, the source region and drain region;

depositing a dielectric layer of silicon oxide on the dielectric liner layer;

depositing a bottom anti-reflective coating over the dielectric layer;

depositing a photoresist over the bottom anti-reflective coating;

photolithographically patterning and developing the photoresist to form a photoresist contact opening therein;

etching a tapered opening in the bottom anti-reflective coating using the photoresist contact opening;

etching a tapered contact opening through the dielectric layer to the source and drain regions using the bottom anti-reflective coating;

removing the photoresist;

removing the bottom anti-reflective coating; and

depositing a conductive material in the tapered contact opening to form a contact.

7. The method as claimed in claim 6 including a step of depositing a bottom anti-reflecting coating of silicon oxy-nitride on the dielectric layer before forming the photoresist over the dielectric layer for assisting in the patterning of the photoresist.

8. The method as claimed in claim 6 including depositing a bottom anti-reflective coating of silicon oxy-nitride on the dielectric layer.

9. The method as claimed in claim 6 wherein etching a tapered contact opening uses a semi-isotropic etching process.

10. The method as claimed in claim 6 wherein depositing a conductive material includes: depositing the conductive metal over the dielectric layer and in the tapered contact opening, the conductive metal selected from a group consisting of tungsten, tantalum, titanium, copper, aluminum, gold, silver, alloys thereof, and compounds thereof; and planarizing the conductive metal flush with the dielectric layer.

11. A semiconductor device on a semiconductor substrate, comprising:

a multi-layer structure on an active region on the semiconductor substrate;

sidewall spacers around the multi-layer structure;

a dielectric layer over the semiconductor substrate, including the multi-layer structure, the sidewall spacers, and the active region having a tapered contact opening provided therein; and

a conductive material in the tapered contact opening to form a contact in contact with the active region.

12. The semiconductor device as claimed in claim 11 wherein the conductive metal is from a group consisting of tungsten, tantalum, titanium, copper, aluminum, gold, silver, alloys thereof, and compounds thereof.

13. A semiconductor device on a semiconductor substrate, comprising:

a multi-layer structure on an active region on the semiconductor substrate;

sidewall spacers around the multi-layer structure;

source and drain regions in the active region adjacent the sidewall spacers;

a dielectric liner layer of silicon nitride over the semiconductor substrate, in contact with the multi-layer structure, the sidewall spacers, the source region and drain region;

a dielectric layer of silicon oxide on the dielectric liner layer having a tapered contact opening through the dielectric layer to the source and drain regions using the bottom anti-reflective coating; and

a conductive material in the tapered contact opening to form a tapered contact.

14. The semiconductor device as claimed in claim 13 wherein the conductive metal is from a group consisting of tungsten, tantalum, titanium, copper, aluminum, gold, silver, alloys thereof, and compounds thereof.